Experimental Investigations on Pulsed-Neutron-induced Single Event Upset Bursts in Commercial ECC SRAMs

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ISINN26, Xi'An
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Overview

- ☐ **Introduction**
  - ● Neutron-induced single event upset
  - ● Initiative of this work
- ☐ **Pulsed neutron experiments**
  - ● Experiment setup
  - ● Experimental results
- ☐ **Interpretation using MBU distribution model**
  - ● MBU distribution model
  - ● Improvement for ECC
  - ● Calculation results and discussion
- ☐ **Conclusion**

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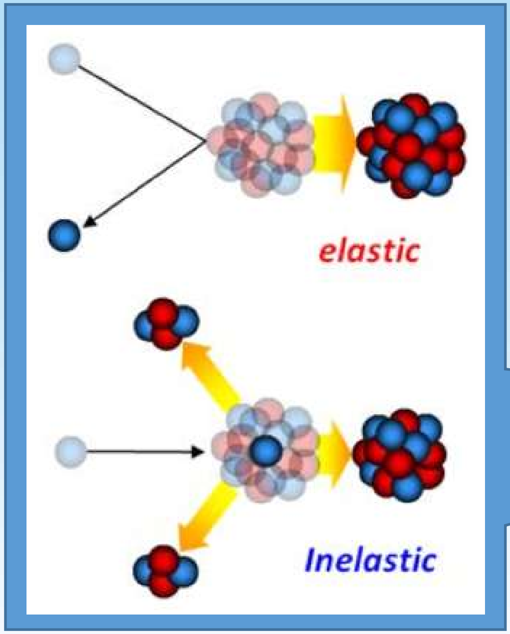
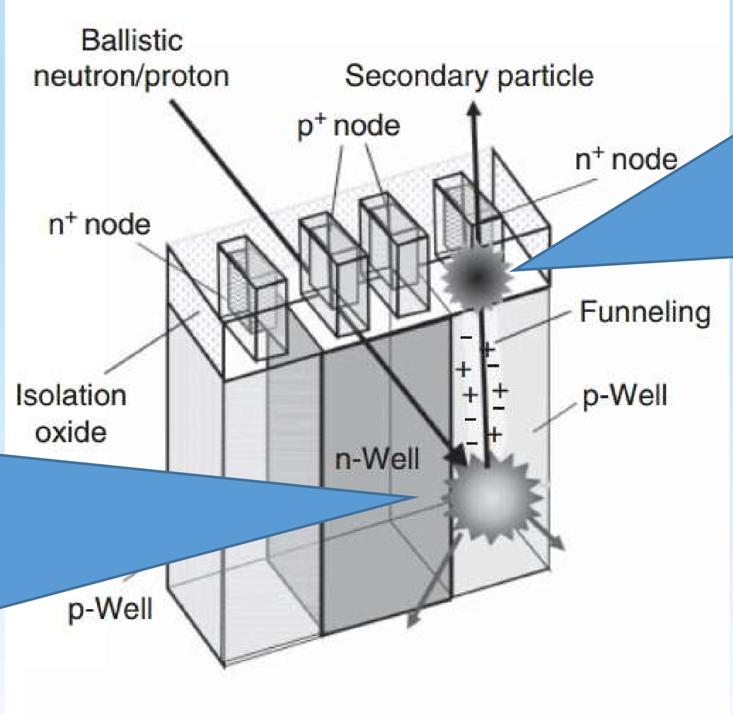
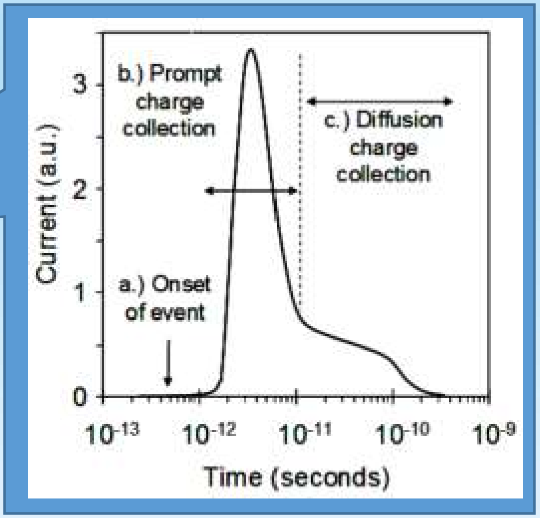
Neutron-induced single event upset

- Neutrons interact with nuclei to produce charged secondary particles – Si recoils, protons, alpha particles…
- Ionizing secondary particles deposit bursts of e-h pairs in electronic devices that may be collected at p-n junctions and produce a current spike that alters data and leads to a digital error.







Ibe, Eishi H. "Terrestrial Radiation Effects in ULSI Devices and Electronic Systems." Wiley, 2014.
Robert Baumann, "Landmarks in Terrestrial Single-Event Effects,"Part B of the Short Course presented at NSREC, 8 July 2013.

Impacts of NSEU

BIG Business Impact

Sun Screen

Daniel Lyons, *Forbes Global*, 11.13.00

mysterious glitch has been popping up since late last year... for America Online, Ebay and dozens of other major corporate accounts...The SUN (server) has caused crashes at dozens of customer sites. An odd problem involving **stray cosmic rays and memory chips** in the flagship Enterprise server line...

A dotcom company bought a Sun 6500 server to run...the core of its business. The server crashed and rebooted four times over a few months. **"It's ridiculous. I've got a $300,000 server that doesn't work. The thing should be bulletproof,"** says the company's president.

Loss of customer confidence = Loss of revenue

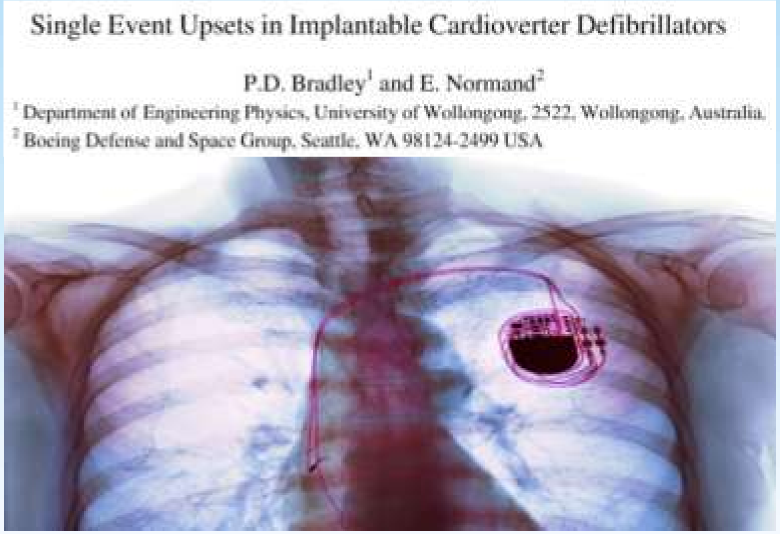
ASCI Q-Machine at Los Alamos National Laboratory

One neutron can stop a calculation

Safety Impact: QANTAS Flight 72

"In-flight upset, 154 km west of Learmonth, WA, 7 Oct. 2008, VH-QPA Airbus A330-303," ATSB Transp. Safety Report – Aviation Occurrence Invest., AO-2008-070, pp. 1 – 313, Dec. 2011.

Single subatomic event has human-scale impact!



Single Event Upsets in Implantable Cardioverter Defibrillators

P.D. Bradley[1] and E. Normand[2]

[1] Department of Engineering Physics, University of Wollongong, 2522, Wollongong, Australia.

[2] Boeing Defense and Space Group, Seattle, WA 98124-2499 USA

Robert Baumann, "Industrial Challenges and Trends in Terrestrial Single-Event Effects", TI Information – Selective Disclosure, October, 2014.
Steve Wender, "Neutron-Induced Failures in Semiconductor Devices", WPI Seminar, LA-UR-14-23043, May, 2014.
Michael Gordon, "Single Event Upsets and Microelectronics (Why neutrons matter to the electronics industry)", Neutron Monitor Community Workshop, October, 2015

Evaluation of NSEU sensitivity

- ☐ **NSEU cross section per bit**

[redacted]

  - ✓ **Fabrication technology and device geometry design**
  - ✓ **Neutron energy spectrum**

- ☐ **Linearity between SEU number and fluence / SEU rate and flux**

$$N_{observed} = \sigma N \Phi$$

[redacted] σN

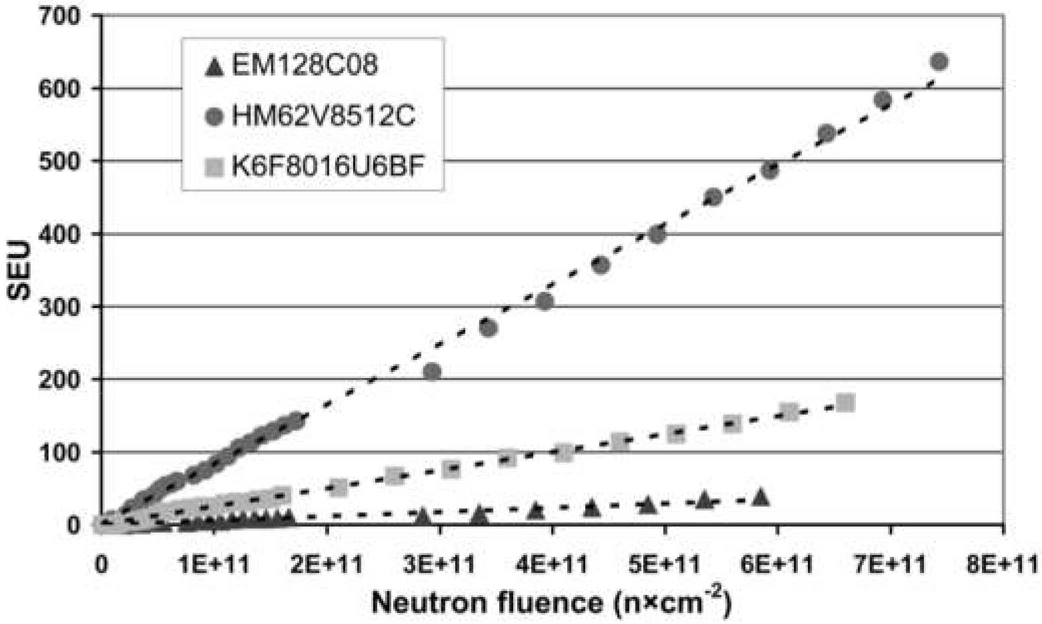


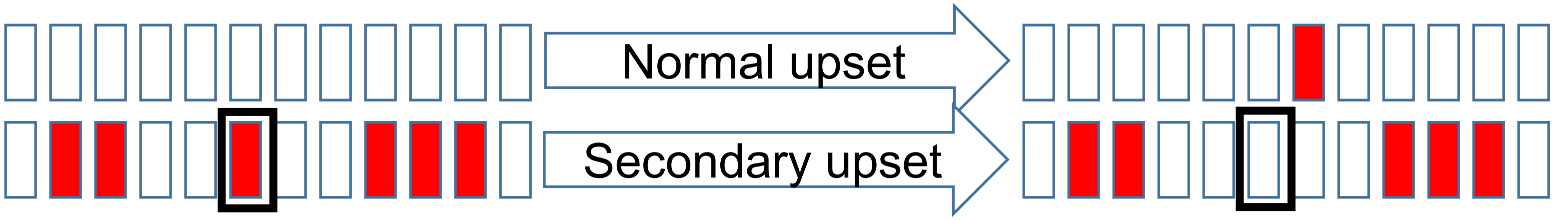
TABLE IV
CROSS SECTIONS OF MEMORIES IRRADIATED WITH FAST NEUTRONS

Reference	Manufacturer	Cross section ($cm^2 \cdot bit^{-1}$)
K6F8016U6BEF	SAMSUNG	$4.8 \cdot 10^{-16}$
HM62V8512C	HITACHI	$1.6 \cdot 10^{-15}$
EM128C08	NANOAMP	$1.1 \cdot 10^{-16}$

J. M. Armani, G. Simon and P. Poirot, "Low-energy neutron sensitivity of recent generation SRAMs," in IEEE Transactions on Nuclear Science, vol. 51, no. 5, pp. 2811-2816, Oct. 2004.

Influence of $\dot{\Phi}T$

- ☐ **Linearity breaks down if $\dot{\Phi}T$ is too high.**
- ☐ **Cause of nonlinearity: secondary upsets**

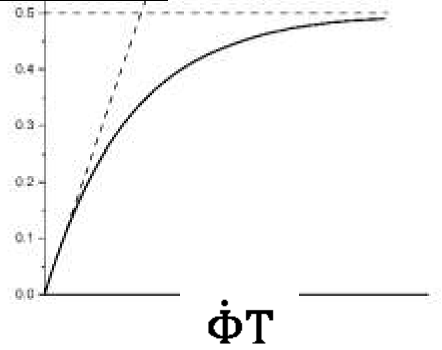


- ☐ **From the test point of view: missing of upset events**

$$\sigma_{observed} = \frac{N_{observed}}{N\dot{\Phi}T} < \sigma_{real} = \frac{N_{real}}{N\dot{\Phi}T}$$

- ☐ **JEDEC JESD89A suggests:**
  - ✓ **Low flux**
  - ✓ **High operating frequency**
  - ✓ **Small $\dot{\Phi}T$**

[redacted]



JEDEC JESD89A. Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray Induced Soft Errors in Semiconductor Devices, JEDEC, 2006.

Initiative of this work

- ☐ **Application: electronics operating in high neutron-flux environment**
  - ✓ **Controlling electronic system of pulsed reactors**
  - ✓ **Peripheral processing circuits of detectors**
  - ✓ **Large $\dot{\Phi}T$ value**
- ☐ **A wide range of fault-tolerant techniques are commonly used in memory circuits, MCUs, FPGAs, et al., correcting upsets effectively under small $\dot{\Phi}T$ conditions**
  - ✓ **ECC (Error Correction Code)**
  - ✓ **TMR(Triple Module Redundancy)**
- ☐ **Evaluation results with traditional small $\dot{\Phi}T$ test conditions tend to overestimate the reliability under pulsed neutron irradiation with high $\dot{\Phi}T$.**

- ● ***Investigate NSEU characteristics of ECC SRAMs experimentally under different $\dot{\Phi}T$ using pulsed neutrons.***
- ● ***More importantly, find out the relationship between NSEU and $\dot{\Phi}T$ and its root cause to help comprehend the experimental results.***

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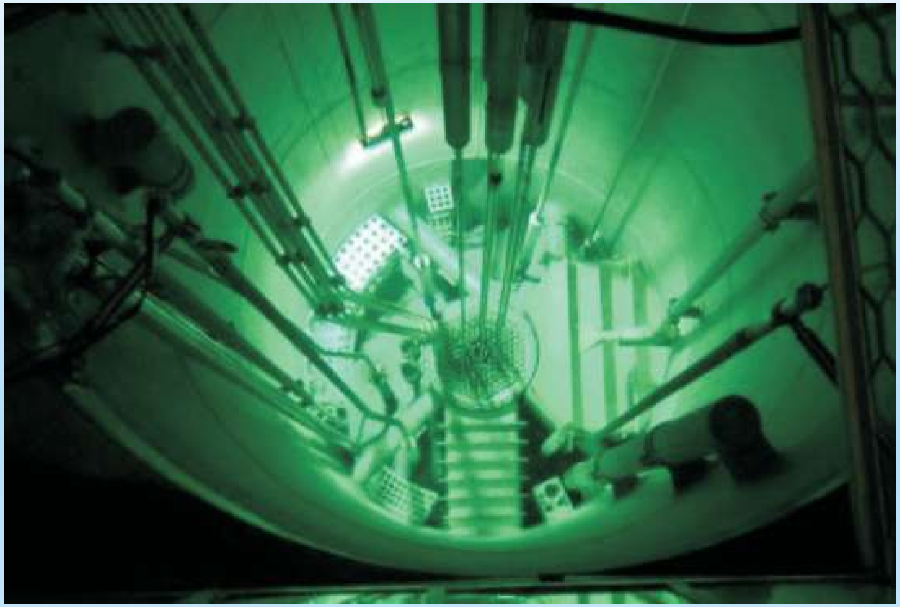
Experiment setup - radiation field



- ☐ **Xi'An Pulsed Reactor (XAPR)**
  - ✓ No. 3 Irradiation Chamber
  - ✓ Fast neutrons with mean neutron energy of approximately 1 MeV

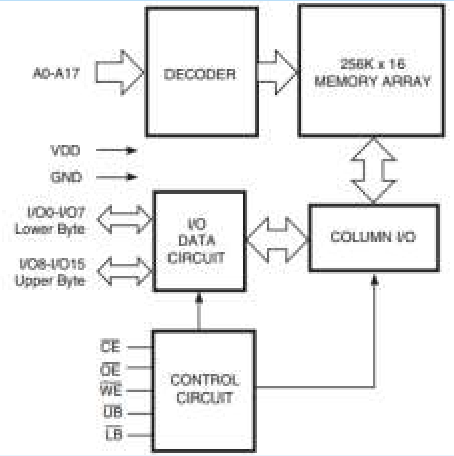
$\dot{\Phi}T$

[redacted]

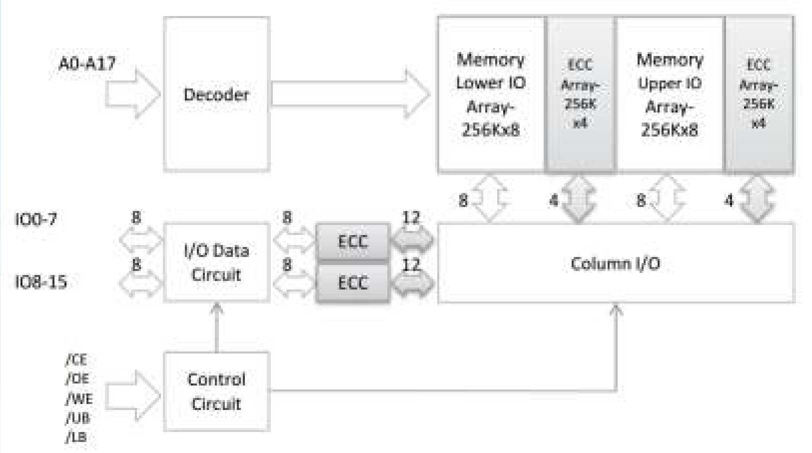
Shot No.	Reactivity / dimensionless	FWHM / ms	Peak Neutron Flux / n-cm^{-2}-s $^{-1}$(1-MeV-eqv.)	Neutron Fluence / n-cm^{-2}(1-MeV-eqv.)
1-4	3.2	9.8	7.42×10^{14}	8.32×10^{12}
5	2.0	15.3	2.86×10^{14}	4.71×10^{12}

Experiment setup - devices under test

- 2 models of SRAMs from same family, same vendor
  - ✓ 4 Mbit, 65 nm CMOS technology
  - ✓ Suggests equal σ_{real}
- Only difference: ECC and non-ECC version
  - ✓ Additional ECC circuits and check code memory array for ECC version
  - ✓ 2 samples for each version: ECC-0 / ECC-1 / non-ECC-0 / non-ECC-1 installed on one single PCB of 10 cm x 10 cm
  - ✓ Neutron fluence variation among different devices < 10%



ISS64WV25616BLL (non-ECC version)



ISSI61WV25616EDBLL (ECC version)

Experiment setup - test method

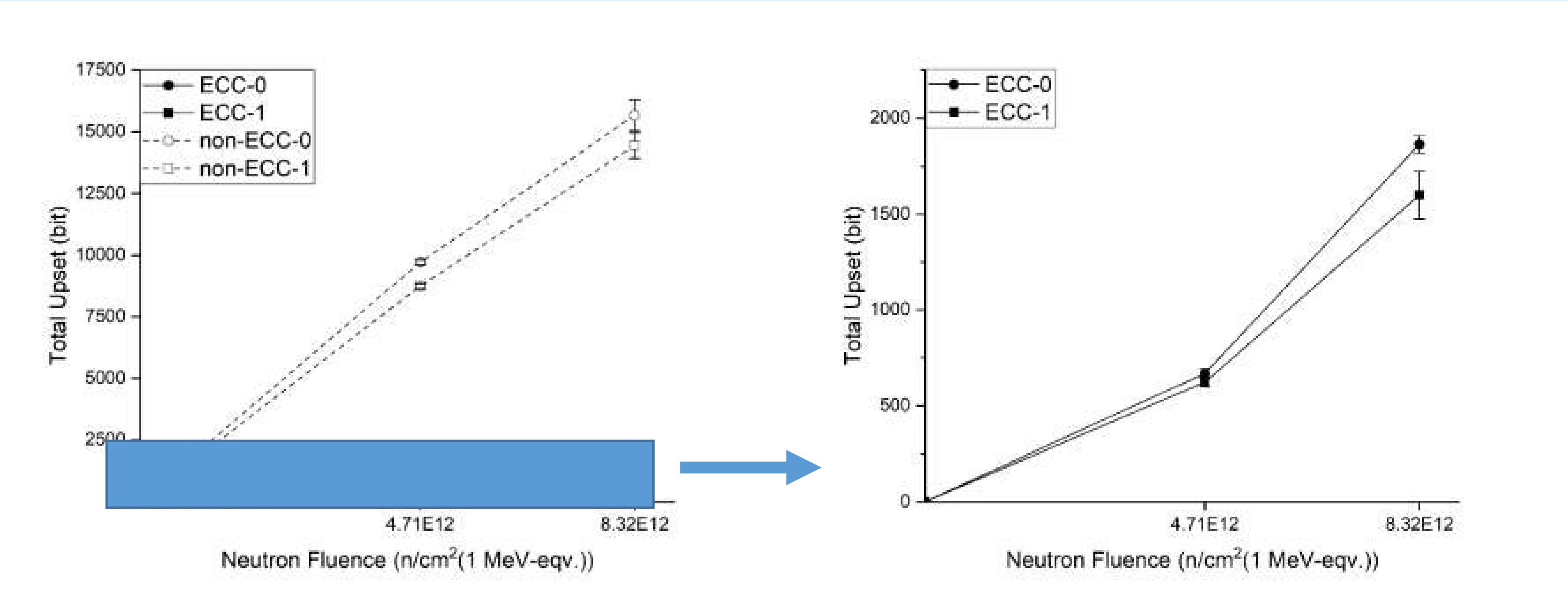
- ☐ **Test system**
  - ✓ Customed SRAM test system executes writing and reading operations to DUTs (Devices Under Test)
  - ✓ Communicate with a laptop via a USB cable

- ☐ **Bias condition**
  - ✓ One single 3.3 V power supply for all the 4 samples

- ☐ **Test procedure**
  - ✓ DUTs filled with 0x 55H into all the addresses before irradiation and stay static during neutron pulse
  - ✓ Test system reads back the data from the DUTs immediately after the neutron pulse and obtains the statistical information
  - ✓ Statistical information contains total upset number, byte numbers for SBU, 2-bit MBU and 3-bit MBU

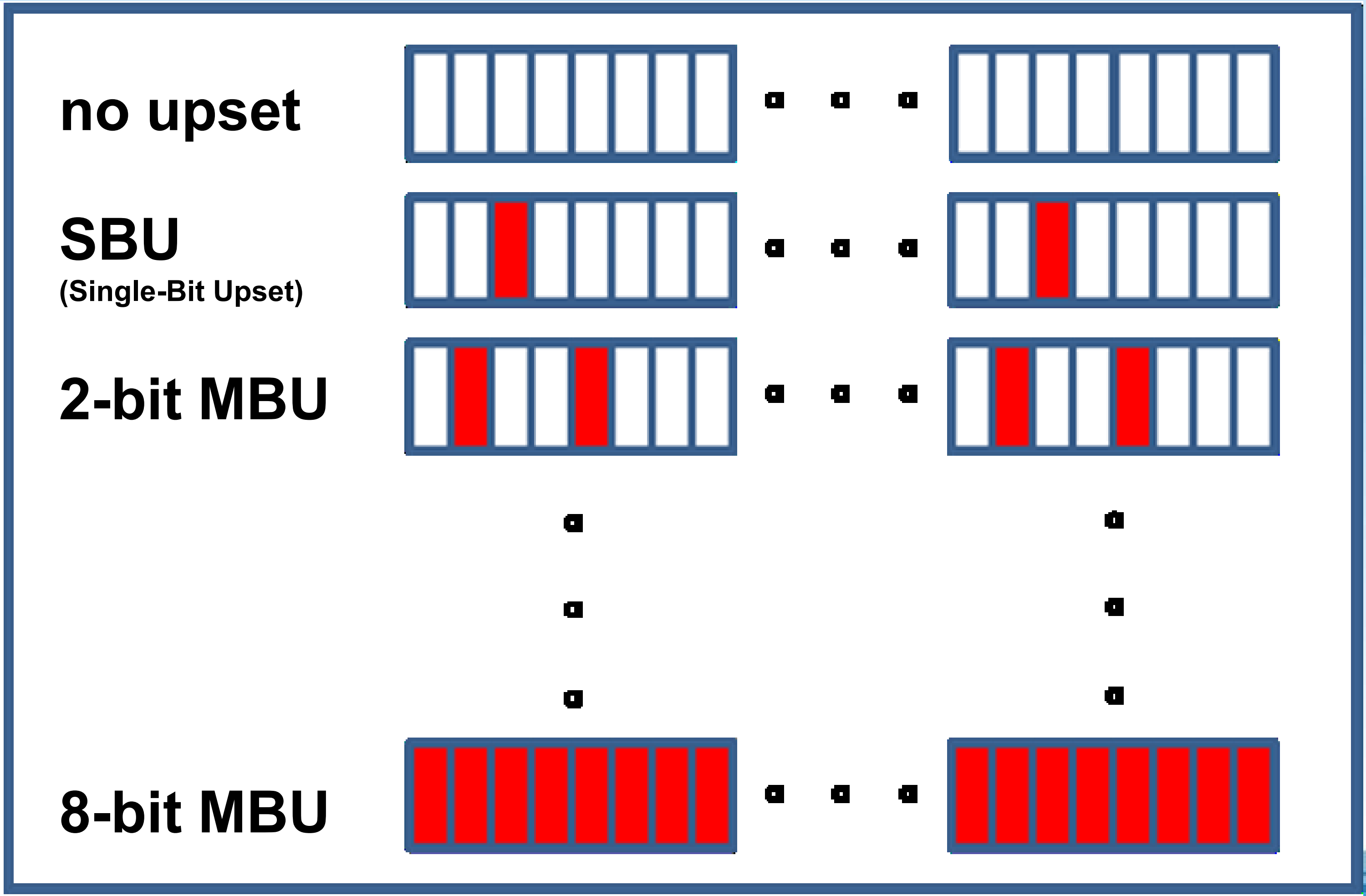
Experimental results – NSEU vs Φt

- **Impact of ECC operations on NSEU:**
  - ✓ **ECC SRAMs manifested far more less upsets (~1 order of magnitude)**
- **Linearity:**
  - ✓ **Non-ECC SRAMs: slightly sub-linearity**
  - ✓ **ECC SRAMs: significant super-linearity**



Experimental results - MBU distribution

- MBU (Multiple-Bit Upset within one single byte)
  - ✓ Byte classification
  - ✓ MBU Distribution: (n0, n1, …, n8)



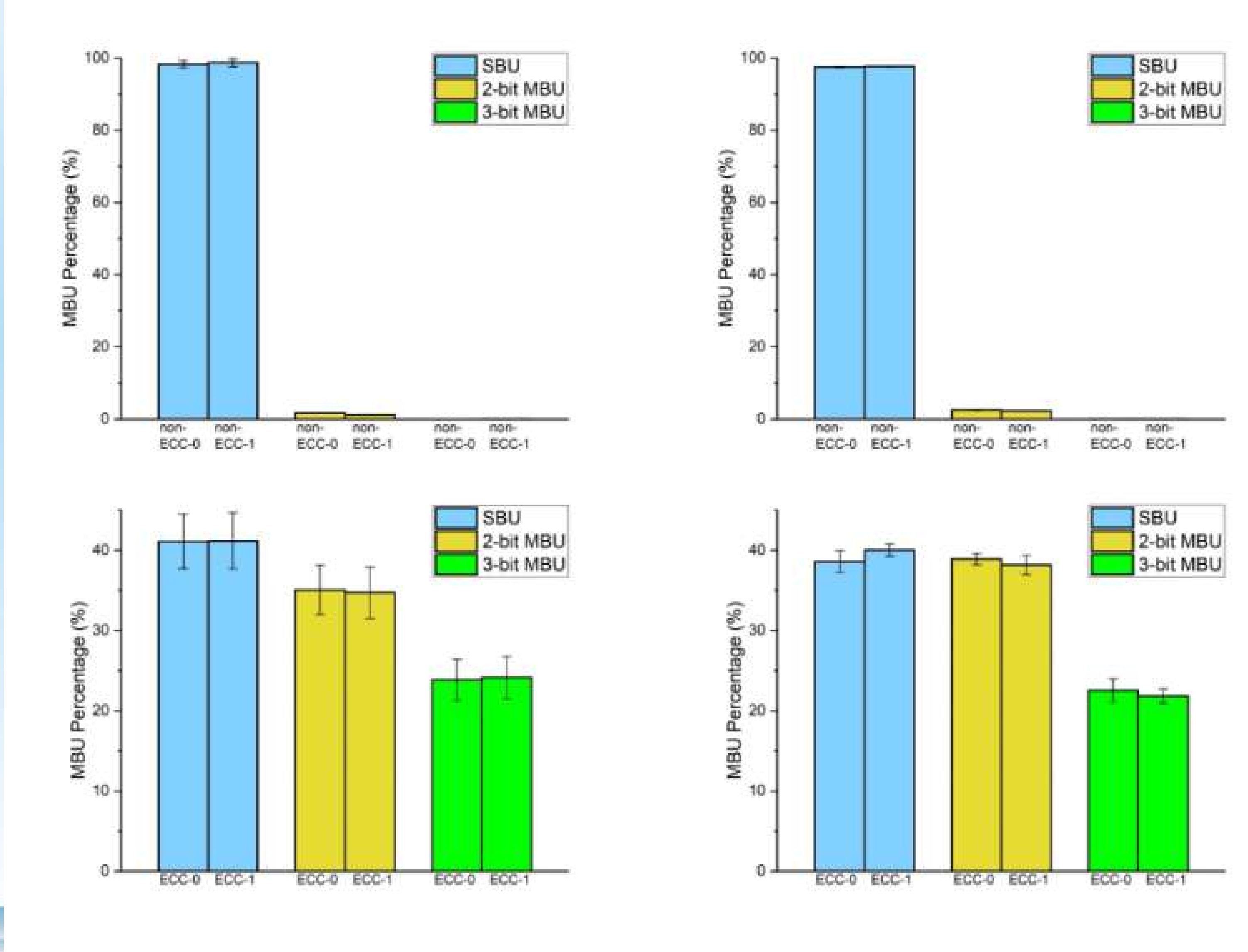
Experimental results - MBU distribution

$\dot{\Phi}T = 4.71E12\ \mathrm{n/cm^2}$

$\dot{\Phi}T = 8.32E12\ \mathrm{n/cm^2}$

non-ECC SRAMs

ECC SRAMs



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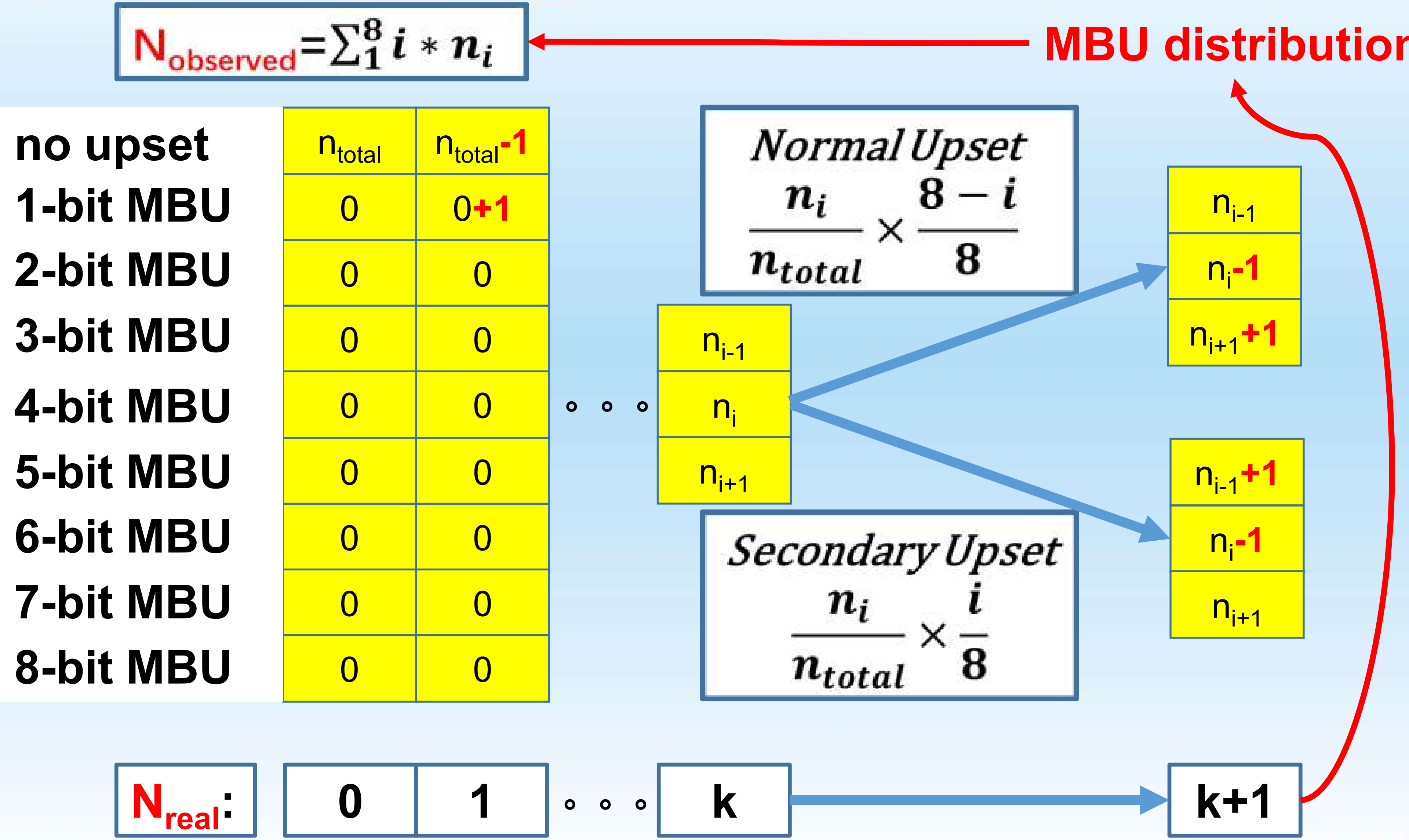
$\overline{N_{observed}}(\dot{\Phi}T) = \overline{N_{observed}}(\overline{N_{real}})$



$N_{observed} = \sum_{1}^{8} i * n_i$

MBU distributio

no upset	n_{total}	n_{total}**-1**
1-bit MBU	0	0**+1**
2-bit MBU	0	0
3-bit MBU	0	0
4-bit MBU	0	0
5-bit MBU	0	0
6-bit MBU	0	0
7-bit MBU	0	0
8-bit MBU	0	0

∘ ∘ ∘

n_{i-1}
n_i
n_{i+1}

Normal Upset

$$\frac{n_i}{n_{total}} \times \frac{8-i}{8}$$

n_{i-1}
n_i**-1**
n_{i+1}**+1**

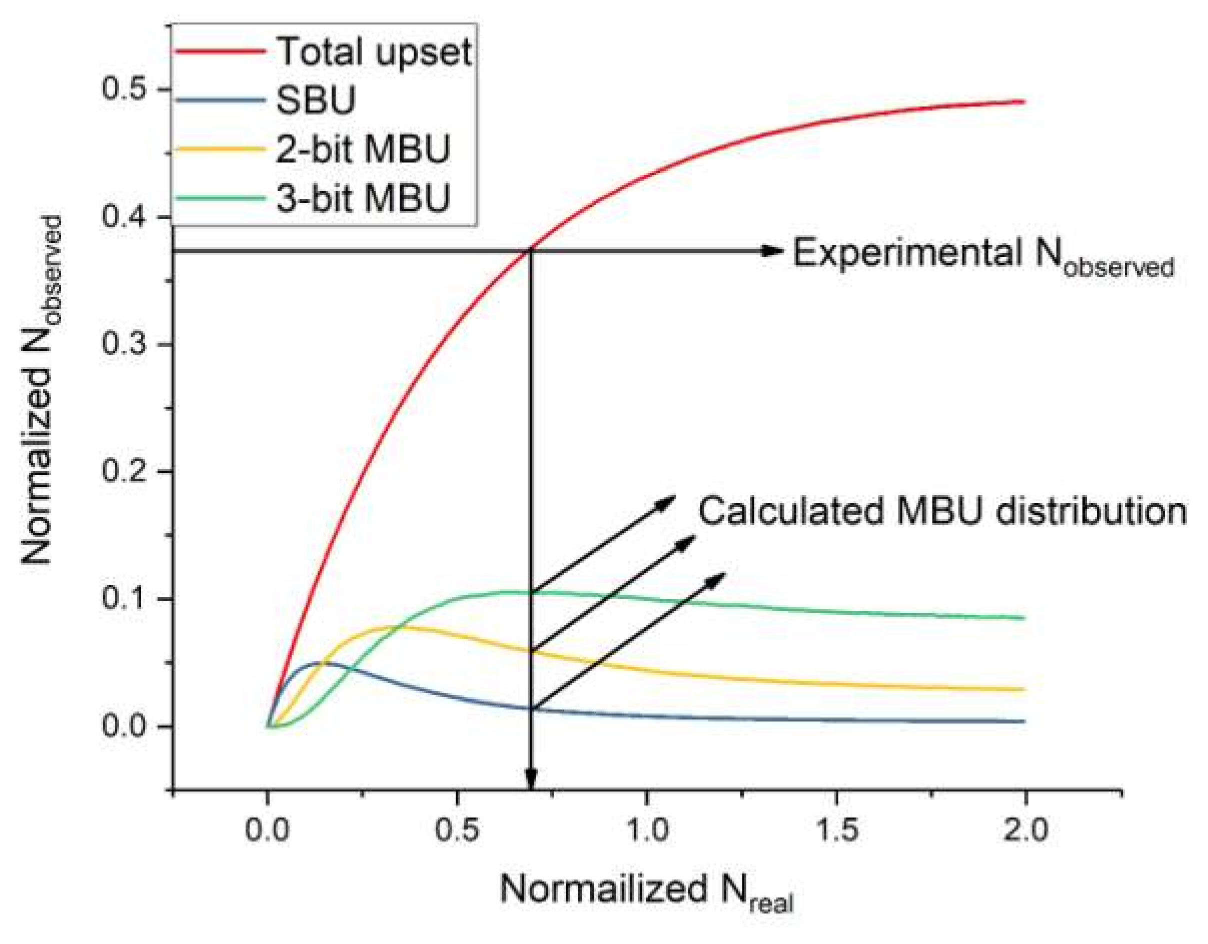
Secondary Upset

$$\frac{n_i}{n_{total}} \times \frac{i}{8}$$

n_{i-1}**+1**
n_i**-1**
n_{i+1}

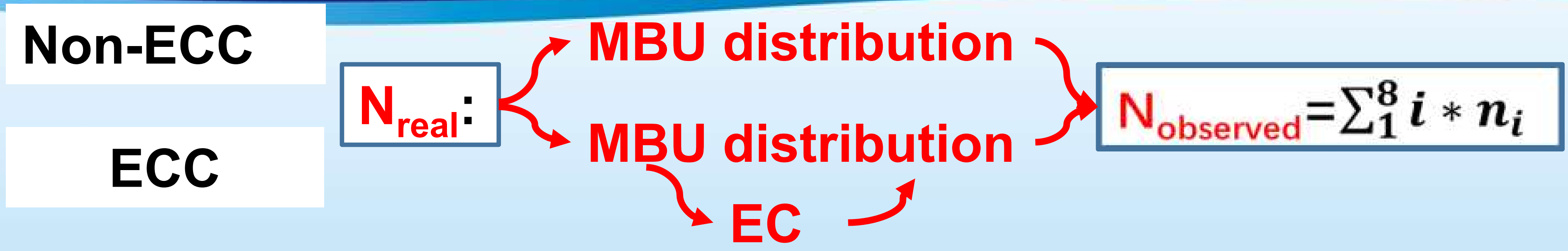
N_{real}:	0	1	∘ ∘ ∘	k	→	k+1

Verification of MBU distribution model



MBU distribution model for non-ECC SRAMs

Improvement for ECC



Non-ECC

ECC

N_{real}:

MBU distribution

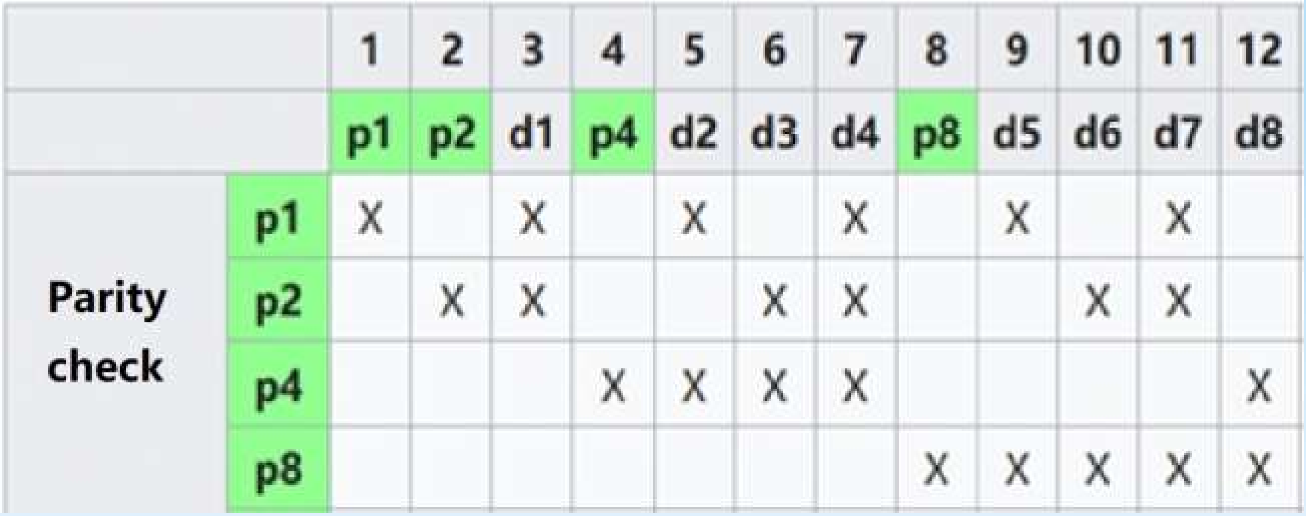
MBU distribution

ECC

$N_{observed}=\sum_1^8 i * n_i$

- ☐ How MBU distribution is changed by ECC

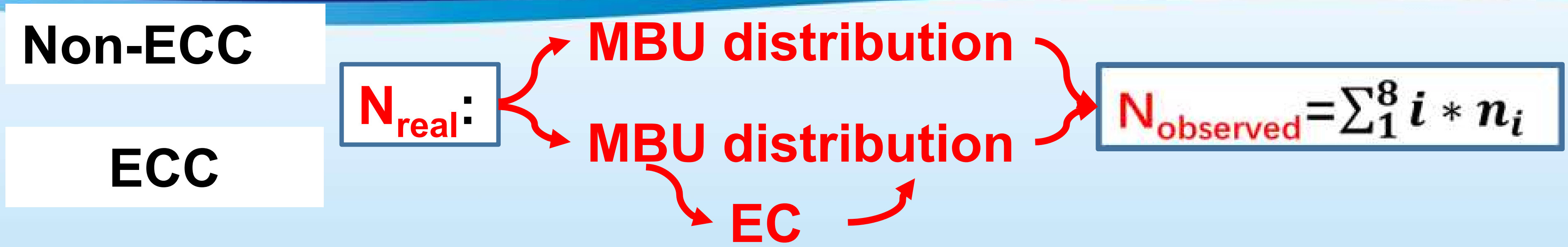
no upset	n_0
1-bit MBU	n_1
2-bit MBU	n_2
3-bit MBU	n_3
4-bit MBU	n_4
5-bit MBU	n_5
6-bit MBU	n_6
7-bit MBU	n_7
8-bit MBU	n_8



		1	2	3	4	5	6	7	8	9	10	11	12
		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity check	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

[p1, p2, p4, p8]

Improvement for ECC



Non-ECC

ECC

N_{real}:

MBU distribution

MBU distribution

ECC

$N_{observed}=\sum_{1}^{8} i * n_i$

- ☐ How MBU distribution is changed by ECC

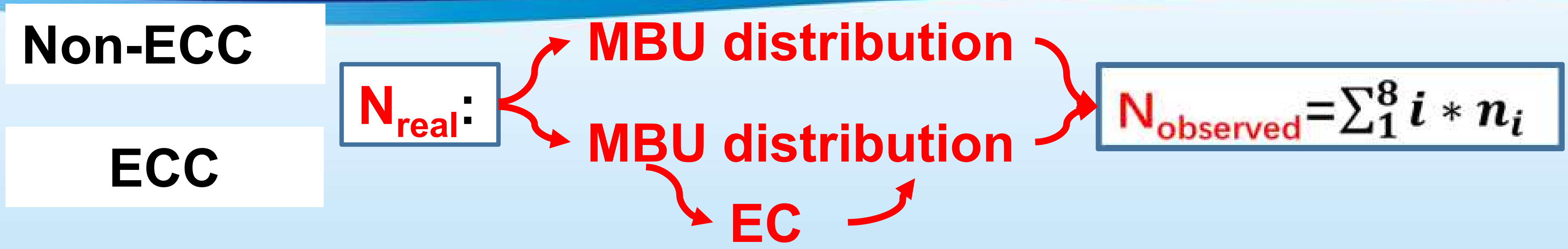
no upset	n_0+1
1-bit MBU	n_1-1
2-bit MBU	n_2
3-bit MBU	n_3
4-bit MBU	n_4
5-bit MBU	n_5
6-bit MBU	n_6
7-bit MBU	n_7
8-bit MBU	n_8

		1	2	3	4	5	6	7	8	9	10	11	12
		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity check	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

[p1, p2, p4, p8] =[1, 0, 1, 0]→d2 is upset

SBU → no upset

Improvement for ECC



- ☐ How MBU distribution is changed by ECC

no upset	n_0
1-bit MBU	n_1
2-bit MBU	n_2-1
3-bit MBU	n_3+1
4-bit MBU	n_4
5-bit MBU	n_5
6-bit MBU	n_6
7-bit MBU	n_7
8-bit MBU	n_8

		1	2	3	4	5	6	7	8	9	10	11	12
		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity check	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

[p1, p2, p4, p8] =[1, 1, 1, 0]→d4 is upset

2-bit MBU → 3-bit MBU

Improvement for ECC

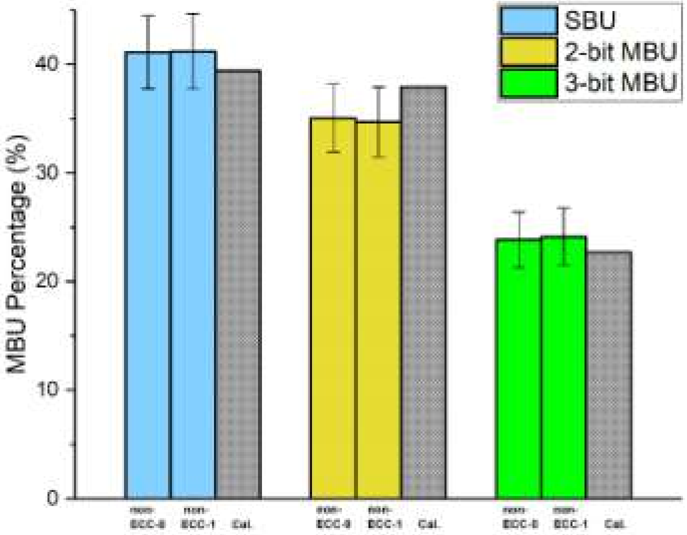
- **Exhaustion calculation results (ECC Transforming Matrix)**

MBU bytes before ECC correction	Percentage of MBU bytes after ECC correction								
	0	1	2	3	4	5	6	7	8
1	**1**	0	0	0	0	0	0	0	0
2	0	**0.394**	**0.379**	**0.227**	0	0	0	0	0
3	0.009	0.109	0.382	0.409	0.091	0	0	0	0
4	0.002	0.125	0.255	0.366	0.232	0.020	0	0	0
5	0	0.020	0.184	0.369	0.306	0.106	0.015	0	0
6	0	0	0.053	0.220	0.422	0.242	0.055	0.008	0
7	0	0	0.023	0.114	0.290	0.383	0.167	0.023	0
8	0	0	0	0.051	0.232	0.372	0.246	0.099	0
9	0	0	0	0	0.037	0.382	0.445	0.091	0.045
10	0	0	0	0	0	0.091	0.409	0.470	0.030
11	0	0	0	0	0	0	0.500	0.167	0.333
12	0	0	0	0	0	0	0	1	0

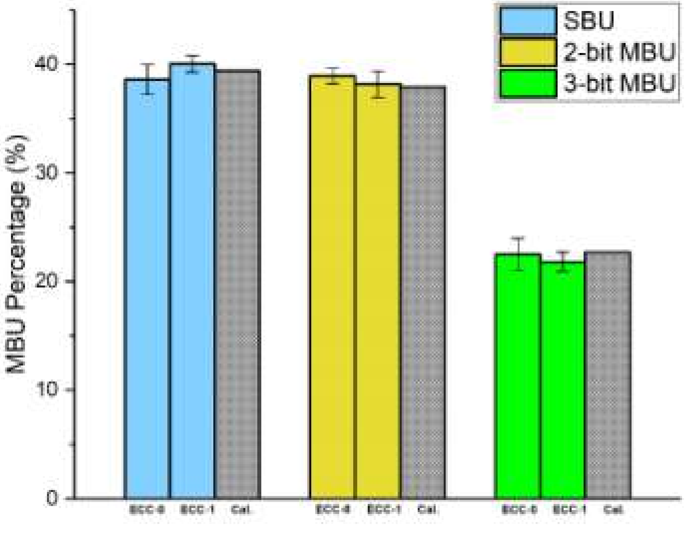
MBU distribution

- MBU distribution of ECC SRAMs: experiment VS calculation

$\dot{\Phi}T = 4.71E12$ n/cm^2



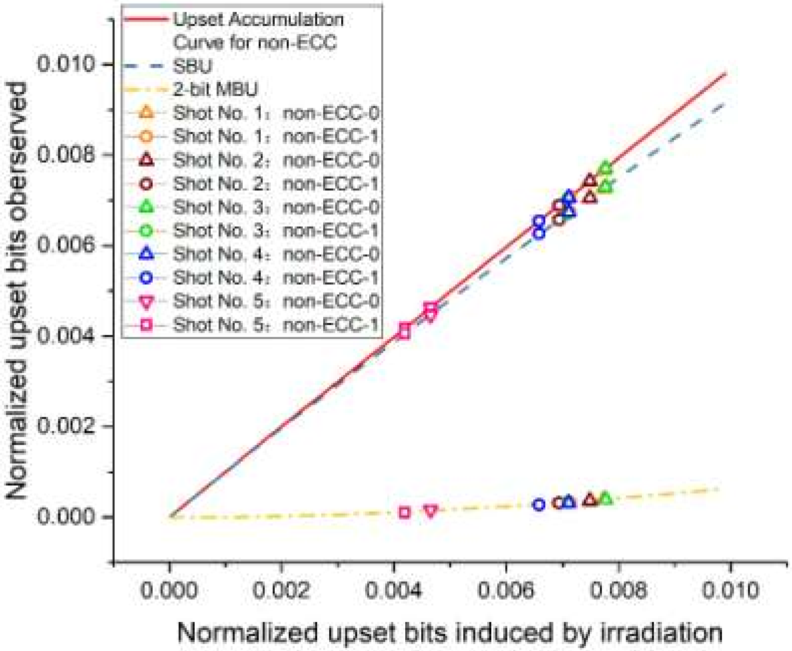
$\dot{\Phi}T = 8.32E12$ n/cm^2

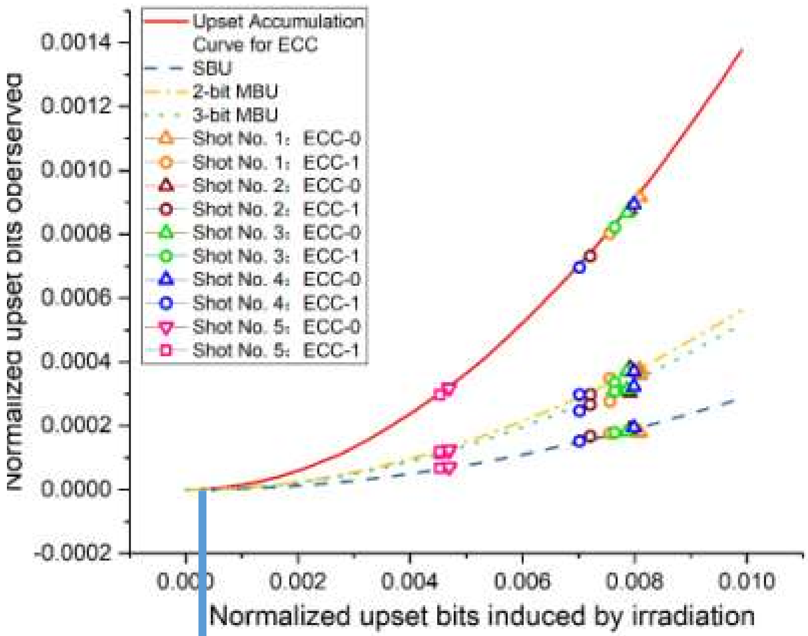


- Perfectly consistent
- New MBU distribution model is established

Calculation results and verification

- **Calculated $\overline{N_{observed}}$ ($\overline{N_{real}}$) VS Experiment results**

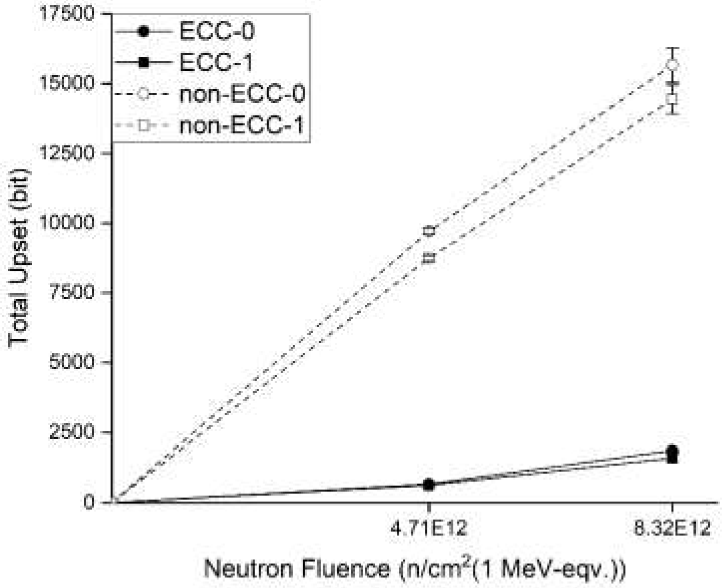




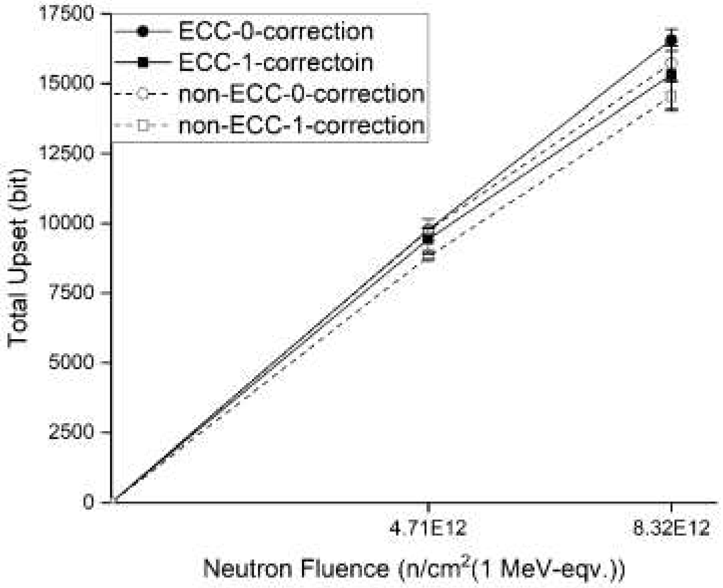
Small $\dot{\Phi}T$, typically 2-3 orders of magnitude lower than the pulsed neutron

Correcting NSEU vs ϕT

- ☐ $\overline{N_{observed}}$ ($\overline{N_{real}}$)
- ☐ **Similar slopes indicate the same σ_{real} for both ECC and non-ECC SRAMs**



Before correction



After correction

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Conclusion

- $\overline{N_{observed}}$ ($\overline{N_{real}}$)
    - ✓ MBU distribution is handled as a bridge to connect $\overline{N_{observed}}$ with its corresponding $\overline{N_{real}}$
    - ✓ In addition, ECC transforming matrix should be applied for ECC SRAMs
    - ✓ Perfectly agrees with the experimental results
- Results of ECC SRAMs evaluated with low neutron flux could significantly underestimate the sensitivity under pulsed neutron irradiation due to the difference in $\dot{\Phi}T$.
- To accurately evaluate the NSEU sensitivity of ECC SRAMs, large $\dot{\Phi}T$ should be applied in order to obtain statistically valid data.

Thanks for your attention!

ISINN26, Xi'An

June 1st, 2018